NANOVEA
Affiliate of Micro Photonics Inc.

SILICON WAFER FLATNESS
WITH 3D METROLOGY

Prepared by
Benjamin Mell

6 Morgan, Ste156, Irvine CA 92618 · P: 949.461.9292 · F: 949.461.9232 ·nanovea.com
Micro Photonics Inc."16 Years of Excellence"

INTRO:

A wafer is a thin piece of semiconductor material, which is used in microelectronic device and integrated circuit production. Silicon crystal is an example of a semiconductor material. The wafer acts as the substrate for the micro-devices that are fabricated in, and over, the wafer. Doping or ion implantation, photolithographic patterning, deposition of different materials, and etching are all examples of the many micro-fabrication process steps a wafer can go through.

WAFER FABRICATION CONCERNS

Wafer flatness has a very large influence on silicon wafers because of the impact it can have on the ability of photolithographic systems to effectively print circuit features. A specific area of the wafer is exposed to a circuit image by steppers, which then step to a neighboring area and replicate this procedure until the whole wafer has been exposed. In order to eliminate the dependence on wafer flatness, current steppers tilt the wafer and then focus the image when exposing each particular area. Severe changes in surface topography within the area of exposure, however, can alter the circuit feature image and, ultimately, lead to potential die yield loss.

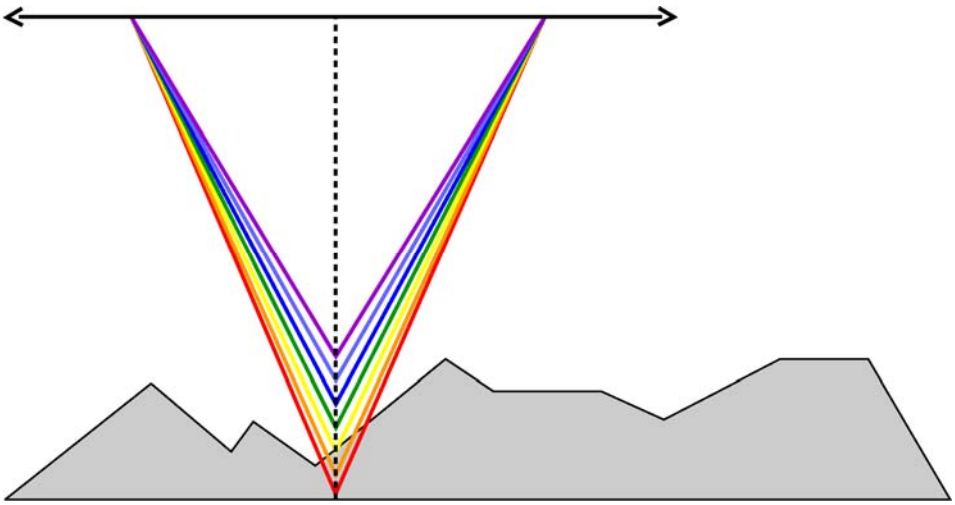
MEASUREMENT OBJECTIVE

Manufacturing engineers, in an effort to diminish die yield loss, indicate a maximum allowable peak-to-valley surface height range for silicon wafers. However, unsuitable peak-to-valley specifications can bring about increased cost for the industry. Silicon wafer manufacturers use surface topography measurement and inspection instruments, capable of measuring the specified flatness range, to determine if a wafer is able to be sold a prime market price or if it should be downgraded or discarded completely.

In this application, the CR750 is used to measure the surface topography of a silicon wafer. By measuring the topography of the wafer, the maximum peak-to-valley height change can be calculated, which is the parameter if interest for silicon wafer suppliers in determining the value of the wafer. Quality control by these means could reveal impending die yield loss in the future.

MEASUREMENT PRINCIPLE:

The axial chromatism technique uses a white light source, where light passes through an objective lens with a high degree of chromatic aberration. The refractive index of the objective lens will vary in relation to the wavelength of the light. In effect, each separate wavelength of the incident white light will re-focus at a different distance from the lens (different height). When the measured sample is within the range of possible heights, a single monochromatic point will be focalized to form the image. Due to the confocal configuration of the system, only the focused wavelength will pass through the spatial filter with high efficiency, thus causing all other wavelengths to be out of focus.

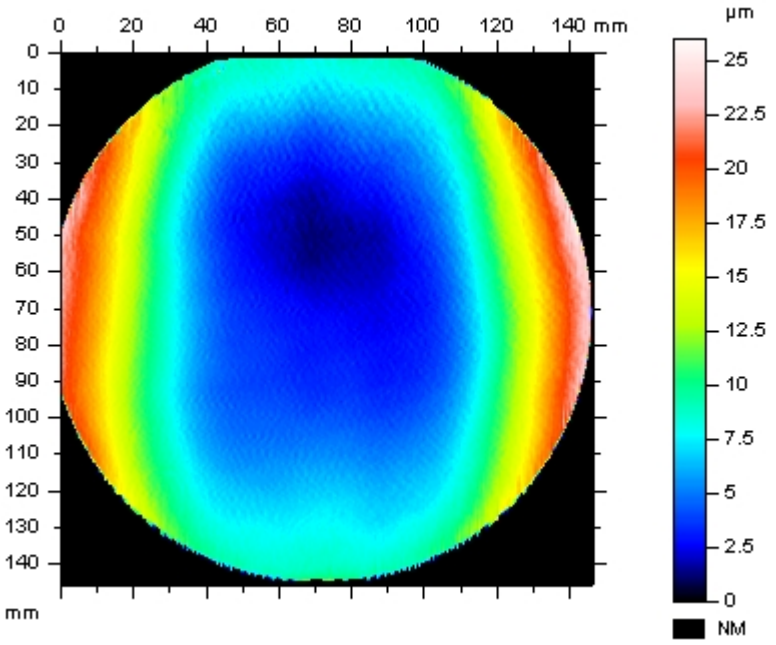


The spectral analysis is done using a diffraction grating. This technique deviates each wavelength at a different position, intercepting a line of CCD, which in turn indicates the position of the maximum intensity and allows direct correspondence to the Z height position.

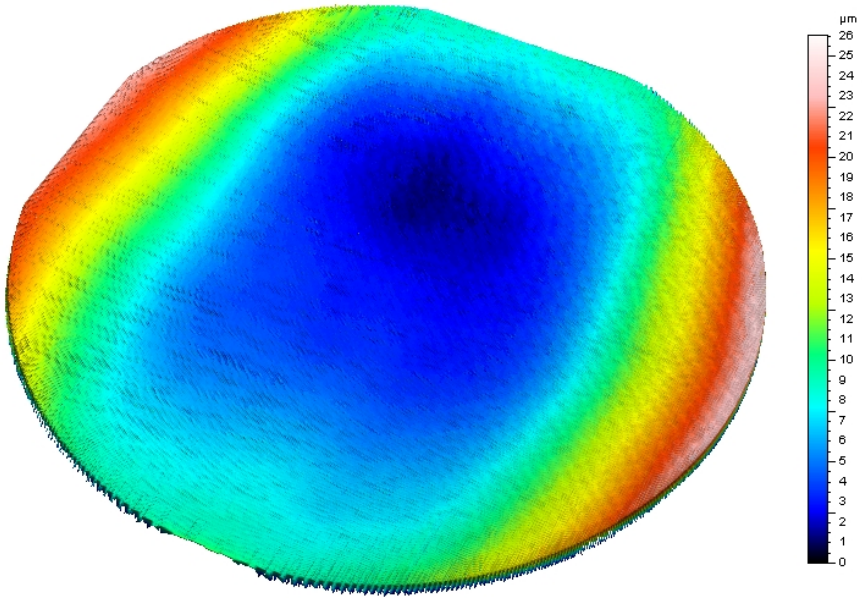
TEST RESULTS:

FLATNESS CALCULATIONS

FLATNESS PARAMETER		DEFINITION
FLTt	26.03 µm	*Peak-to-Valley Flatness Deviation of the Surface*
FLTp	17.49 µm	*Peak-to-Reference Flatness Deviation of the Surface*
FLTv	8.538 µm	*Reference-to-Valley Flatness Deviation of the Surface*
FLTq	5.427 µm	*Root Mean Square Flatness Deviation of the Surface*



2-D False Color Height Representation of Wafer in Nanovea 3D Analysis Software



3-D False Color Height Representation of Wafer in Nanovea 3D Analysis Software

TEST DISCUSSION:

The essential peak-to-valley height difference for the measured wafer is 26.03 µm. The specified maximum allowable peak-to-valley surface height range for the wafer in this study is unknown. However, this parameter is quickly and easily computed using the Nanovea CR750 and its analysis software.

CONCLUSION:

The Nanovea CR750 can be used to accurately measure the surface topography of silicon wafers, from which surface flatness deviation calculations can be made. The full wafer surface can be measured quickly and accurately due to the versatile measurement technique used by the CR750. Using the measurement data, the analysis software provided with the CR750 can produce flatness parameter values that can be used to verify that a given wafer is in compliance with peak-to-valley height range the manufacturer has specified. As previously mentioned, this type of quality control can help decrease possible die yield loss and wafer rejection resulting from excessive wafer bow, curvature, or waviness. When properly instituted, wafer flatness metrology provides useful information that can produce improved wafer processing capabilities.